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REISSUE PATENT APPLICATION TRANSMITTAL

Address to:
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Box Patent Application
Washington, DC 20231

Attorney Docket No.	501.20289RC6
First Named Inventor	Hisashi Maejima
Original Patent Number	5,230,747
Original Patent Issue Date (Month/Day/Year)	July 27, 1993
Express Mail Label No.	

JC914 U.S. PTO 09/704529 11/03/00

APPLICATION FOR REISSUE OF: (check applicable box) [X] Utility Patent [ ] Design Patent [ ] Plant Patent

APPLICATION ELEMENTS

1. [X] * Fee Transmittal Form *(PTO/SB/56)* *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification and Claims *(amended, if appropriate)*
3. [X] Drawing(s) *(proposed amendments, if appropriate)* (9 sheets)
4. [X] Reissue Oath / Declaration (original or copy) *(37 C.F.R. § 1.175)(PTO/SB/51 or 52)*
5. Original U.S. Patent
   - [X] Offer to Surrender Original Patent *(37 C.F.R. § 1.178)* *(PTO/SB/53 or PTO/SB/54)*
   - *or*
   - [ ] Ribboned Original Patent Grant
   - [ ] Affidavit / Declaration of Loss *(PTO/SB/55)*
6. Original U.S. Patent currently assigned?
   - [X] Yes [ ] No
   - *(If Yes, check applicable box(es))*
   - [X] Written Consent of all Assignees *(PTO/SB/53 or 54)*
   - [ ] 37 C.F.R. § 3.73(b) Statement [ ] Power of Attorney

ACCOMPANYING APPLICATION PARTS

7. [X] Foreign Priority Claim *(35 U.S.C. 119)* *(if applicable)*
8. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
9. [ ] English Translation of Reissue Oath/Declaration *(if applicable)*
10. [ ] * *Small Entity* Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard *(MPEP 503)* *(Should be specifically itemized)*
13. [X] Other: Credit Card Payment Form
    Request for Transfer of Drawings

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Signature	Ronald J. Shore	Date	Nov. 3, 2000

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REISSUE APPLICATION FEE TRANSMITTAL FORM

Docket Number (Optional): 501.20289RC6

JC914 U.S. PTO 09/714529 11/03/00

Claims as Filed - Part 1

Claims in Patent	For	Number Filed in Reissue Application	(3) Number Extra	Small Entity Rate	Small Entity Fee		Other than a Small Entity Rate	Other than a Small Entity Fee
(A) 20	Total Claims (37 CFR 1.16(j))	(B) 12	**** 0 =	x $___ =		or	x $ 18 =	0
(C) 3	Independent Claims (37 CFR 1.16(i))	(D) 3	* 0 =	x $___ =			x $ 80 =	0
	Basic Fee (37 CFR 1.16(h))				$			$ 710
	Total Filing Fee				$		OR	$ 710

Claims as Amended - Part 2

	(1) Claims Remaining After Amendment		(2) Highest Number Previously Paid For	(3) Extra Claims Present	Small Entity Rate	Small Entity Fee		Other than a Small Entity Rate	Other than a Small Entity Fee
Total Claims (37 CFR 1.16(j))	***	MINUS	**	* =	x $___ =		or	x $___ =	
Independent Claims (37 CFR 1.16(i))	***	MINUS	*****	=	x $___ =			x $___ =	
			Total Additional Fee			$		OR	$

* If the entry in (D) is less than the entry in (C), Write "0" in column 3.
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Signature of Applicant, Attorney or Agent of Record

Ronald J. Shore (Reg. No. 28,577)
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REISSUE APPLICATION FEE TRANSMITTAL FORM

Docket Number (Optional)
501.20289RC6

Claims as Filed - Part 1

Claims in Patent	For	Number Filed in Reissue Application	(3) Number Extra	Small Entity Rate	Small Entity Fee		Other than a Small Entity Rate	Other than a Small Entity Fee
(A) 20	Total Claims (37 CFR 1.16(j))	(B) 12	**** 0 =	x $____ =		or	x $ 18 =	0
(C) 3	Independent Claims (37 CFR 1.16(i))	(D) 3	* 0 =	x $____ =			x $ 80 =	0
				Basic Fee (37 CFR 1.16(h))	$____			$ 710
				Total Filing Fee	$		OR	$ 710

Claims as Amended - Part 2

	(1) Claims Remaining After Amendment		(2) Highest Number Previously Paid For	(3) Extra Claims Present	Small Entity Rate	Small Entity Fee		Other than a Small Entity Rate	Other than a Small Entity Fee
Total Claims (37 CFR 1.16(j))	***	MINUS	**	* =	x $____ =		or	x $____ =	
Independent Claims (37 CFR 1.16(i))	***	MINUS	*****	=	x $____ =			x $____ =	
				Total Additional Fee	$			OR	$

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WAFER HAVING CHAMFERED BEND PORTIONS IN THE JOINT REGIONS BETWEEN THE CONTOUR OF THE WAFER AND THE CUT-AWAY PORTION OF THE WAFER

This is a continuation application of application Ser. No. 07/240,806 filed Sep. 7, 1988 and now abandoned which, in turn, is a divisional application of application Ser. No. 830,754 filed Feb. 19, 1986, now U.S. Pat. No. 4,783,225 issued Nov. 8, 1988, which, in turn, is a continuation application of application Ser. No. 741,107 filed Jun. 4, 1985, now abandoned, which, in turn, is a continuation application of application Ser. No. 517,405 filed Jul. 26, 1983, now abandoned.

BACKGROUND OF THE INVENTION

The present invention relates to a wafer and a method of working the same and, more particularly, to a novel wafer and method of working the same which can prevent defects such as the chipping of the joint regions between the contour of the wafer and the cut-away portion of the wafer such as an orientation flatness.

In general, in the production of a semiconductor device such as a transistor, an integrated circuit (IC) or a large-scale integrated circuit (LSI), when foreign matter including dust, chipping etc. adhere on the surface of a wafer, which is a substantially circular flat member made of a semiconductor material such as silicon (Si), when subjecting the wafer to processing such as diffusion, coating with a resist, etching and evaporation, the foreign matter causes scratches in the wafer surface and defects such as an nonuniform film thickness and drawbacks arise during transportation of the semiconductor device.

There are various causes for the appearance of such foreign matter. As one of the causes, it has been known that, for example, during the transportation of wafers the outer peripheral part of the wafer collides against any transport mechanism or the wafers come into contact with each other, whereby the outer peripheral part of the wafer itself breaks off locally. Chips resulting from the breakage adhere on the surface of the wafer as the foreign matter, to incur various defects. In order to prevent the aforementioned breakage of the outer peripheral part of the wafer, in, for example, Japanese Patent Application Publication No. 53-38594, both the major surfaces of the wafer outer-peripheral part have been chamfered by mechanical or chemical means.

However, it has been have found that, even when both the major surfaces of the wafer outer-peripheral part are chamfered in this manner, the wafer nevertheless frequently chips.

As a result of research efforts into the cause of chipping, important facts have been revealed. In general, a wafer is formed with a flat portion called the "orientation flatness (principal flatness)" by cutting a part of the wafer rectilinearly, in order to indicate the crystal orientation of the wafer and also to position the wafer. The formation of such flat portion, however, results in forming acute bends in the joint parts between the flat portion and the contour of the wafer. Consequently, the joint part is liable to chipping. That is, during the transportation of the wafer, the joint part collides against the guide of an air bearing or comes into touch with another wafer, whereby this joint part breaks off to give rise to chipping.

As described above, the acute bends are formed in the joint parts between the flat portion as the orientation flatness and the contour of the wafer. In this regard, it has been found that a harmful phenomena occurs in the regions of the acute bends. In the processing of the wafer, when a photoresist film for a photolithographic process is formed on the surface of the wafer, crowns and fringes appear in the photoresist film. When a thin film such as an epitaxially vapor-grown layer is formed on the wafer surface, a film of abnormal thickness is formed due to, e.g., abnormal growth.

It is accordingly an object of the present invention to provide a wafer and a method of working the same which can prevent the appearance of foreign matter and the occurrence of other various defects attributed to the chipping of the joint regions between the contour of the wafer and the cut-away portion of the wafer such as an orientation flatness.

This invention can best be understood by reference to the following description taken in connection with the accompanying illustrative drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view showing a semiconductor wafer which is an embodiment of the present invention;

FIG. 2 is a sectional view taken along line II—II in FIG. 1;

FIG. 3 is an enlarged view of FIG. 2;

FIG. 4 is an explanatory view for illustrating the positioning of wafers;

FIG. 5 is a plan view for explaining the determination of chamfer regions in the wafer shown in FIGS. 1 to 3;

FIG. 6 is a plan view of another embodiment of the wafer according to the present invention;

FIG. 7 is a plan view showing still another embodiment of the present invention;

FIG. 8 is a sectional view taken along line VIII—VIII in FIG. 7; and

FIGS. 9 to 17 are schematic views showing three examples of chamfering devices which can be used for performing a method of working a wafer according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now, the present invention will be described in detail in connection with embodiments illustrated in the drawings.

Referring now to the drawings wherein like reference numerals are used throughout the various views to designate like parts and, more particularly, to FIGS. 1-3, according to these figures, a wafer 1 of this embodiment has a circular shape prepared by, for example, slicing an ingot of silicon (Si) whose sectional shape is substantially circular. In a part of the wafer 1, a principal flatness (flat) or orientation flatness or orientation flat (0. F.) 2 is formed to be rectilinear as a positioning removal portion for indicating the direction of a crystal axis and for positioning the wafer 1 in various processing. As shown most clearly in FIG. 3, an outer peripheral portion 3 of the wafer 1 is, for example, arcuately chamfered.

Further, according to the wafer 1 of this embodiment, in the joint parts 4 between both the ends of the orientation flatness 2 and the contour of the wafer 1, corner regions indicated by two-dot chain lines are chamfered into the shape of circular arcs indicated by solid lines. Due to such structure, the wafer 1 is so

constructed that the corner regions of the joint parts **4** are prevented from chipping during the various processing of the wafer **1**, the chipping causing defects such as the appearance of foreign matter in the form of broken chipping pieces.

More specifically, the chamfered region **5** of the joint part **4** in the embodiment of FIG. **1** is a region enclosed with the solid line and the two-dot chain line. The inner edge of the chamfered region **5** is defined by the circular arc of a common inscribed circle which is inscribed on the contour of the wafer **1** and the orientation flatness **2**.

In case of performing the arcuate chamfering of the joint part **4**, the preferable chamfer range of the chamfered region **5** is determined in a way to be described in detail below with reference to FIGS. **4** and **5**.

The wafers **1** are usually positioned by rotating them while the peripheries of the wafers **1** are held in touch with a roller **6**. Herein, the phenomenon is exploited in which, when the orientation flatness **2** of the wafer **1** has moved up to the roller **6**, the wafer **1** stops rotating due to this orientation flatness being the flat portion.

When the circular periphery of the wafer **1** is in touch with the roller **6**, the wafer **1** is rotated along with the rotation of the roller **6**. With the orientation flatness **2**, however, even when the wafer **1** and the roller **6** lie in touch, the turning effort of the roller **6** does not contribute to the rotation of the wafer **1**. Thus, in spite of the rotation of the roller **6**, the wafer **1** stops rotating and moving and holds its state.

As shown most clearly in FIG. **4**, a wafer jig **100**, receiving a large number of wafers **1**, is placed on a positioning rest **101** which has two rollers **6**. When the rollers **6** are subsequently rotated, the wafers **1** received in the wafer jig **100** start rotating. When the orientation flatness portions **2** of the respective wafers have moved up to the positions of the rollers **6**, the wafers **1** do not rotate any longer and such a state is established for all the wafers **1**. Eventually, all the wafers **1** are aligned in the state in which the orientation flatness portions **2** of the respective wafers **1** are located on the lower side.

In executing such positioning, regulation or alignment of the wafers **1**, there are various methods other then the aforementioned one, such as, for example, a method employing a single roller **6** and a method resorting to optical means composed of photoelectric elements etc.

Referring to FIG. **5**, a wafer **1** having a width W has a radius R, and its center is O_1. The distance from the center 0_1, to the orientation flatness **2** of the wafer is denoted by y.

When a perpendicular is drawn from the center O_1 down to the orientation flatness **2**, the point of intersection P is supposed to be the middle point of the orientation flatness **2**. The reference character b represents a distance between a point at the middle of the full length of the orientation flatness **2** before the chamfer, namely, the point P and a joint part **4** formed by the orientation flatness **2** and the contour of the wafer **1**.

It is stipulated in SEMI standards that the relationship between the length of the orientation flatness **2** as well as the width W of the wafer **1** and the diameter D=2R of the wafer **1** becomes as indicated in Table 1 in the mirror wafer state.

Table 1

	Diameter of Wafer			
	3 inches	100 mm	125 mm	150 mm
Allowable Range of Diameter [mm]	75.56–76.84	±1	±1	±1
Width [μm]	360–410	500–550	600–650	650–700
Length of Orientation Flatness	19.05–25.40	30–35	40–45	55–60

On the other hand, since the wafers **1** need to be positioned by utilizing the orientation flatnesses **2**, the orientation flatness **2** has that length of the flat portion which must be possessed, at the minimum, for accurate positioning. Letting a denote the half of such length, the length a is the distance from the point P to the point of inscription i_1 between a common inscribed circle and the orientation flatness **2**. As noted above, photoelectric elements etc. other than the roller **6** may well be used as the positioning means.

Letting i_2 denote the point of inscription between the common inscribed circle and the contour of the wafer **1**, the center O_2 of the common inscribed circle lies on a straight line which connects the center O_1 of the wafer **1** and the point inscription i_2. The angle between this straight line and the straight line $\overline{O_1P}$ is expressed by θ.

Accordingly, the radius r of the common inscribed circle which is inscribed to both the contour of the wafer **1** and the orientation flatness **2** is obtained as stated below.

First, the minimum required length for the positioning by the rollers **6**, namely, the length a ($a=\overline{Pi_1}$) of that flat portion in the orientation flatness **2** which is not chamfered is given by:

$$a=(R-r)\sin\theta \tag{1}$$

Secondly, the length y of the perpendicular $\overline{O_1P}$ drawn from the center O_1 of the wafer **1** to the orientation flatness **2** is given by:

$$y=(R-r)\cos\theta+r \tag{2}$$

From a right-angled triangle O_1P4, $y^2=R^2-b^2$ holds. Therefore,

$$y=\sqrt{R^2-b^2} \tag{3}$$

Substituting Equation (3) into Equation (2),

$$\sqrt{R^2-b^2}=(R-r)\cos\theta=r \tag{4}$$

$$\cos\theta=\frac{\sqrt{R^2-b^2}-r}{(R-r)}$$

From Equation (1),

$$\sin\theta=\frac{a}{(R-r)} \tag{5}$$

Since $\sin^2\theta+\cos^2\theta=1$, Equations (4) and (5) yield:

$$\frac{a^2}{(R-r)^2}+\frac{(\sqrt{R^2-b^2}-r)^2}{(R-r)^2}=1 \tag{6}$$

Putting Equation (6) in order.

$$r = \frac{b^2 - a^2}{2\,(R - \sqrt{R^2 - b^2})} \tag{7}$$

Accordingly, in the present embodiment, the chamfer region 5 in the joint region 4 between the contour the wafer 1 and the orientation flatness 2 may be worked along the circular arc of any radius as long as this circular arc is the arc of the common inscribed circle radius r in Equation (7) or falls within a region outside it, as indicated by oblique lines in FIG. 5.

That is, the radius r of the inscribed circle common to both the contour line of the wafer 1 and the orientation flatness 2 may lie within a range given by the following expression, and the joint part 4 may be arcuately chamfered within this range of radius r:

$$r \leqq \frac{b^2 - a^2}{2\,(R - \sqrt{R^2 - b^2})} \tag{8}$$

On the other hand, the minimum value of the radius r in the chamfering can be set as stated below.

As shown in FIG. 3, the silicon wafer 1 according to the present invention has the peripheral parts of both its major surfaces chamfered. The dimensions of the chamfering, namely, the length A of a slant face portion and the length B an end face portion are manipulated from experimental values. It was experimentally determined that the length B of the chamfer end face portion differs depending upon the width of the wafer 1. It has been experimentally found that when the length B of is at most 0.32 mm (320 μm) and at least 0.15 mm (150 μm) for W of 0.4 mm, the chipping of the peripheral part the wafer exhibits the minimum value. It has also been found that the chipping of the peripheral part the wafer exhibits the minimum value when 150 μm≦B≦420 μm for W=0.5 mm and when 150 μm≦B≦520 μm for W=0.6 mm. That is, the chipping of the peripheral part of the wafer is minimized when the length B of the chamfer end face portion in the wafer periphery is at least 150 μm and, at most, a value obtained by subtracting 80 μm from the wafer width W. In other words, the chipping falls within the range of 150 μm≦B and B≦(W−80) μm. Thus, in the chamfer dimensions of the silicon wafer 1 according to the present invention, the length B of the end face portion is set by the following expression, whereby the breakage and chipping of the wafer 1 attributed to mechanical shocks etc. during the processing or transportation of the wafer extraordinarily decreases:

$$150\ \mu \leqq B \leqq (W-80)\ \mu\text{m} \tag{9}$$

On the other hand, the length A of the slant face portion in the chamfer dimensions of the silicon wafer 1 according to the present invention is experimentally set to be at least 0.2 mm (200 μm), whereby the breakage and chipping of the wafer 1 attributed to mechanical shocks etc. during the processing or transportation of the wafer can be extraordinarily reduced.

In view the above and as shown in FIG. 3, the peripheral parts both the major surfaces of the semiconductor wafer may be chamfered. Herein, the chamfering dimensions as to the sectional shape of the wafer may be such that the length B of the chamfer end face portion is set at a value within the range not smaller than 150

μm and not greater than the value obtained by subtracting 80 μm from the width the wafer, while the length A of the chamfer slant face portion is rendered at least 200 μm.

Accordingly, the radius r of the inscribed circle common to both the contour of the wafer **1** and the orientation flatness **2** may fall within a range given by the following expression, and the joint part may be chamfered arcuately within this range of radius r:

$$\frac{W-B}{2} \leqq r \tag{10}$$

From Expressions (8) and (10), the chamfering radius r may lie within a range given by the following expression:

$$\frac{W-B}{2} \leqq r \leqq \frac{b^2-a^2}{2\left(R-\sqrt{R^2-b^2}\right)} \tag{11}$$

where

r=radius of the wafer chamfering circle,

R=radius of the wafer,

a=half of the length of the unchamfered portion (flat portion) in the wafer cut-away portion,

b=half the full length of the wafer cut-away portion before being chamfered,

W=width of the wafer, and

B=length of the wafer end face portion.

In this manner, the wafer **1** according to the present invention is chamfered in the peripheral parts of the sliced silicon wafer with the predetermined dimensions and is thus smoothed so as not to protrude the corners so that a breaking off or chipping of the wafer is prevented. Moreover, even when there is an impact on the wafer **1**, there is no local concentration of a load, therefore the strength of the peripheral part of the wafer increases, and the quantity of the chipping of the peripheral part can be reduced. Accordingly, it is possible to avoid the problem of silicon chips floating in the air as dust and the adhering of the chips to the surface of the silicon wafer; therefore, in the wafer processing for producing a semiconductor device a photoresist film in a photolithographic process can the external appearance its surface enhanced and a lowering of its resolution prevented, and favorable vapor growth etc. free from any abnormal epitaxial growth can be effected. Further, since the chamfering dimensions are adapted to relieve the crowns and fringes of the photoresist and to enhance the resolution thereof, various patterns can be formed on the wafer by fine working.

According to the present invention, no acute corner or bend exists in the joint region between the contour the wafer **1** and the orientation flatness **2**. Therefore, it is possible to prevent a break off in the joint regior and development of chipping due to, for example, the collision against the guide of an air bearing or contact with another wafer during the transportation the wafer **1**. In addition to the defect of the foreign matter due to the appearance of chip pieces, it is also possible to significantly reduce defects such as, for example, inferior transportation due to acute corner hitches on the guide of the air bearing, etc., and an inferior thickness of a resist film attributed to a partial dispensing of resist film due to the turbulence of an air current in the acute corner during the application of the resist. This is especially favorable for wafers of large diameter.

As shown in FIG. 6, the joint parts 4 between the contour a wafer 1 and an orientation flatness 2 are rectilinearly chamfered within the ranges of chamfer regions 5 indicated by oblique lines. The maximum chamfer range of the chamfer region 5 is defined by a straight line which connects the points of inscription i_1 and i_2 of an inscribed circle common to both the contour of the wafer 1 and the orientation flatness 2, as explained before with reference to FIG. 5. The radius r of the common inscribed circle can be selected within the same range as indicated by expression (11).

Also in FIG. 6, there is no acute corner or bend in the joint part 4 between the contour of the wafer 1 and the orientation flatness 2, so that the defect of the foreign matter due to the appearance of chipping pieces, the defect of the transportation, the defect of the thickness of a resist film, etc. can be sharply reduced.

The chamfering according to the present invention may be in any shapes other than the arcuate and rectilinear shapes in the foregoing embodiments, such as various curved shapes and polygonal shapes insofar as the shapes can remove acute corners.

The present invention is applicable, not only to providing the principal flatness or the orientation flatness, but also to providing a sub flatness or a second flatness. More particularly as illustrated in FIGS. 7 and 8, the chamfer regions 5 of the joint regions between both the ends the orientation flatness 2 and the contour of the wafer 1 are chamfered, and, as in ranges indicated by symbol 5*a*, also the joint regions between both the ends of the second flatness 7 and the contour of the wafer 1 are chamfered along the arcs of common inscribed circles inscribed to both the second flatness 7 and the contour of the wafer 1 or along straight lines connecting the points of inscription of the common inscribed circles, or in the regions outside them.

Further, the present invention is applicable to a case where, besides the flat portions such as the orientation flatness 2 and the second flatness 7, a curved positioning notch 8 is formed in the wafer 1. In this case, the joint regions between both the ends of the positioning notch 8 and the contour of the wafer 1 may be chamfered along the arcs of common inscribed circles inscribed to both the positioning notch 8 and the contour of the wafer 1 or along straight lines connecting the points of inscription of the common inscribed circles, or in the regions outside them, as in ranges indicated by symbol 5*b*.

The chamfering of the present invention may well be performed simultaneously with the formation of the orientation flatness 2, or with the chamfering of the outer peripheral part 3 in the thickness direction. Such simultaneous chamfering is very favorable in point of the job efficiency, but separate chamfering may well be performed. Of course, the present invention does not always require the chamfering of the outer peripheral part 3 of the wafer 1 in the thickness direction.

Examples of chamfering devices for carrying out the necessary chamfering in the wafers described above are illustrated in FIGS. 9 to 13. The devices are so-called shape profiling type devices. While a grindstone 81 having a rectilinear groove 9 is rotated, it is moved in the horizontal direction and the vertical direction to perform a chamfering operation. The grindstone 81 can also perform a chamfering of the outer peripheral part of the wafer 1 in the thickness or width direction. The chamfering device also includes a chuck mechanism 102 for the wafer 1, and a chuck mechanism 103 for the

grindstone **81** which are respectively adapted to rotate and move vertically and horizontally.

FIGS. **14** to **16** provide an example of a so-called shape transfer type chamfering device. While being rotated, a grindstone having a curved groove **11** which is conformed to the shape of the chamfering of the outer peripheral part of the wafer **1**, in the thickness direction, is moved in the horizontal direction. Thus, the outer peripheral part of the wafer **1** can be chamfered as shown in FIGS. **1** to **3**. Additionally, the chamfer regions **5**, **5***a* and **5***b* shown in FIGS. **5** to **8** can be chamfered.

In this manner, the chamfering devices in FIGS. **9** to **16** can perform both the chamfering of the chamfer regions **5**, **5***a*, **5***b* and that of the outer peripheral part of the wafer **1**. Therefore, these mechanical chamfering operations can be efficiently performed at the same time, though they may well be executed individually.

FIG. **17** provides an example of a chemical chamfering device wherein a rotary supporter **12** in which a large number of wafers **1** are sandwiched, is immersed in a liquid etchant **14** (for example, a solution having a composition which consists of fluoric acid, nitric acid and glacial acetic acid at a volumetric ratio of 2:5:3) contained in an etching bath **13**. While being rotated along with the rotary supporter **12**, the wafers **1** have their outer peripheral parts etched by the liquid etchant **14**. In this case, in order to chamfer only the chamfer regions **5**, **5***a* and **5***b*, the other outer peripheral parts the wafers **1** need to be masked so as not to touch the liquid etchant **14**. However, the corners of the whole outer peripheries may well be chemically chamfered in the thickness direction by the liquid etchant after the chamfer regions **5**, **5***a* and **5***b* have been formed by mechanical grinding in advance. In the case of FIG. **17**, mechanical shocks on the wafers **1** can be relieved.

The present invention is not restricted to the wafers made silicon (Si), but is also applicable to wafers made of germanium (Ge) or various compound semiconductor materials such as gallium arsenic (GaAs) and gallium garnet.

As set forth above, according to the present invention, no acute corner or bend exists in the joint regions between the contour of the wafer and the cut-away portion of the wafer such as a removed portion for positioning. It is therefore possible to remarkably reduce defects ascribable to the existence of acute corners or bends, such as the defect of a foreign matter due to the chipping the wafer, the defect of transportation and the defect of the thickness of a resist film.

What is claimed is:

1. A wafer for forming an integrated circuit thereon, the wafer comprising:

a main surface on which an integrated circuit is to be formed;

a substantially circular contour portion surrounding said main surface;

a curved positioning notch formed in said circular contour portion; and

connecting portions defined between said circular contour portion and said curved positioning notch, wherein said connecting portions are chamfered in a plane parallel to said main surface.

2. A wafer according to claim 1, wherein the chamfer of each of said connecting portions lies within the range defined by the points of an inscribed circle common to both the circular contour portion and the curved positioning notch, and a radius of each inscribed circle is determined by the following expression:

$$\frac{w-B}{2} \leq r \leq \frac{b^2-a^2}{2(R-\sqrt{R^2-b^2})}$$

where

r = radius of the inscribed circle,

R = radius of the wafer,

a = half of a length of an unchamfered portion in a positioning removal portion,

b = half of a full length of the positioning removal portion before the chamfering,

W = width of the wafer, and

B = length of wafer end face portion.

[3. A wafer according to claim 1, wherein at least one of said connecting portions is rectilinearly chamfered in a plane parallel to said main surface.]

4. A process for producing a semiconductor device, comprising the steps of:

preparing a wafer having a main surface, a substantially circular contour portion and a curved positioning notch formed in said circular contour portion, said circular contour portion chamfered in a thickness direction to said main surface;

forming a photoresist film for a photolithographic process on said surface of said wafer; and

forming patterns on said surface of said wafer,

wherein connecting portions each defined between said circular contour portion and said curved positioning notch is chamfered in a plane parallel direction to said main surface.

5. A process for producing a semiconductor device according to claim 4, wherein the chamfer of said

connecting portion lies within the range defined by the points of an inscribed circle common to both the circular contour portion and the curved positioning notch.

6. A process for producing a semiconductor device according to claim 5, wherein a radius of said inscribed circle is determined by the following expression:

$$\frac{w-B}{2} \leq r \leq \frac{b^2-a^2}{2(R-\sqrt{R^2-b^2})}$$

where

r = radius of the inscribed circle,

R = radius of the wafer,

a = half of a length of an unchamfered portion in a positioning removal portion,

b = half of a full length of the positioning removal portion before the chamfering,

W = width of the wafer, and

B = length of wafer end face portion.

7. A process for producing a semiconductor device, comprising the steps of:

preparing a wafer having a main surface, a substantially circular contour portion, a curved positioning notch formed in said circular contour portion and connecting portions each defined between said circular contour portion and said curved positioning

notch, said circular contour portion and said connecting portions are chamfered in a plane parallel and in a thickness direction to said main surface;

forming a photoresist film for a photolithographic process on said surface of said wafer; and

forming patterns on said surface of said wafer, wherein said connecting portions are curved shape in said main surface and in a plane parallel to said main surface.

8. A process for producing a semiconductor device according to claim 7, further comprising the step of:

positioning said wafer by rotating said wafer.

9. A process for producing a semiconductor device according to claim 7, further comprising the step of:

positioning said wafer by rotating said wafer in touch with a roller means.

10. A process for producing a semiconductor device according to claim 7, further comprising the step of:

positioning said wafer by optical means.

11. A process for producing a semiconductor device according to claim 7, further comprising the step of:

transporting said wafer.

12. A process for producing a semiconductor device

according to claim 7, wherein the chamfer of said connecting portion lies within the range defined by the points of an inscribed circle common to both the circular contour portion and the curved positioning notch.

13. A process for producing a semiconductor device according to claim 12, wherein a radius of said inscribed circle is determined by the following expression:

$$\frac{w-B}{2} \leqq r \leqq \frac{b^2-a^2}{2(R-\sqrt{R^2-b^2})}$$

where

r = radius of the inscribed circle,

R = radius of the wafer,

a = half of a length of an unchamfered portion in a positioning removal portion,

b = half of a full length of the positioning removal portion before the chamfering,

W = width of the wafer, and

B = length of wafer end face portion.

ABSTRACT

A wafer having chamfered bent portions in the joint regions between the contour of the wafer and the cut-away portion of the wafer such as an orientation flatness. The chipping of the wafer can be prevented, and in coating the wafer with a photoresist, forming an epitaxially grown layer on the wafer, etc., films having desired characteristics can be provided on the surface of the wafer.

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AGENCY FOR INVENTIONS AND PATENTS

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(54) Method for the production of special wafers made from semiconductor material

(57) This invention relates to a production process for wafers, which are used in the manufacture of electronic components; it offers several advantages compared to conventional wafers, particularly in regard to high-temperature treatment and during structuring of the wafers. The object of the invention is therefore to avoid or at least reduce the negative effects of the temperature field during high-temperature treatment, affecting the physical shape of the wafers during lithography. This problem has been solved by notching a grown mono-crystal in an axial direction according to a certain pattern, then slicing it in a direction which is vertical to its axis (alternatively, the sliced wafers can be notched later, preferably in a radial direction; see FIG. 1). The notched wafers obtained by this process are then polished using a suitable technology and are subjected to a production cycle for manufacturing electronic components. This application is primarily intended for large-diameter silicon wafers, which are used for the production of highly-integrated components.

-Fig. 1- 12 pages

Title of the invention

Method for the production of special wafers made from semiconductor material

Field of the invention

This invention relates to a production process for special wafers made from semiconductor material, particularly silicon, which is obtained by a known crystal-growing method in a mono-crystalline, mostly dislocation-free structure and in the form of large cylindrical crystal pieces. Round wafers, having a thickness of some 10^{-1} mm and produced from such crystals, are required for manufacturing electronic components. During the process of manufacturing these electronic components which are usually arranged in large numbers on a single wafer, each wafer is subjected to certain steps of a high-temperature treatment and/or structuring, depending on the technology required for the component.

Description of the Related Art

For economic reasons, these wafers are usually not treated separately in an oxidation or diffusion furnace during the manufacturing process - which would be advantageous in regard to the temperature field - but

are usually arranged in batches, then placed simultaneously in certain intervals in a high-temperature furnace. The wafers are energized by absorbing infrared and visible light from the radiation field of the furnace, whereby the mean temperature of the wafers slowly approaches the temperature of the furnace. During heating and cooling of the wafers a mainly radially oriented heat flow will be created within the wafers, according to the temperature distribution of the wafer; this is caused by the previously described arrangement of the wafers in the furnace. During heating of the wafer, these heat flows are oriented in a negative radial direction, while during cooling they change to a positive radial direction. The prevailing gradients of the temperature field lead to mechanical stress within the wafer, causing harmful effects which increase proportionally with the diameter of the wafer. The larger the diameter of the wafer, the more intense the stress becomes, which has a major influence on the geometric and structural resistance of the wafer. After some high-temperature treatment steps, the wafers are showing structural defects (such as dislocations, stacking faults) in disturbing concentrations and arrangements, as well as lasting deformations, caused by mechanical stress

effects. Several methods have been tried to secure the high-temperature resistance of the wafers, such as special polishing techniques, optimum furnace temperature profiles, defined charging (inserting and removing the wafers to/from the furnace), adding certain doping agents (O, H, B) during crystal growing, as well as low-temperature oxidation. Nevertheless, there is no known fully satisfying solution to the problem of high-temperature resistance on large-diameter wafers.

During lithographic processes, particularly during photolithography, the above mentioned deformations, faults or rough spots on the wafer surface may have a detrimental effect on the sharpness of the image, i.e. the structuring; this applies especially to the contact lithography process. However, the tendency towards a total integration of components not only makes it necessary to maintain the current standard of sharpness, but to improve it. For this reason it becomes more and more troublesome if rough spots and deformations of the wafer occur during one of the technological production steps. The dimensional stability of the wafers during the entire technological production sequence of the high-temperature treatment and/or the lithographic process is - at the current state of technology - by no means guaranteed,

particularly since the demand is rising for wafers with larger diameters. It is for these reasons that this invention uses a different approach.

Object of the invention

It is an object of an invention to develop a method which allows the production of special wafers, made of semiconductor material, which exhibit more advantageous characteristics during high-temperature treatment and during structuring, leading to a significant reduction in rejects by employing this new method.

Summary of the Invention

It is the object of the invention to diminish or eliminate the effects of the temperature field within the volume of the wafers, qualitatively described above, which affects the shape and amount of defects, as well as reducing the defect structure and the negative effects it has on the real shape of the wafers, which influences the structuring sharpness during lithographic processes, particularly during photolithography. This objective is reached in the sense of the invention by employing an innovative manufacturing process for producing special wafers; this process consists largely

of a series of generally known procedure steps used in growing crystals, separating crystals, etching, as well as, for example, temper-hardening, thermal oxidation and/or diffusion. Improved characteristics of the wafers during the production of semiconductor components are obtained by

- growing a basically cylindrical mono-crystal made from semiconductor material by a known crystal-growing method, then making one or more incisions according to a certain system and in an axial direction, from the crystal shell to a certain depth, without cutting completely through the wafer;
- arranging the slit mono-crystal in such a way that it can be cut up at an angle approaching more or less 90° to the axial direction, resulting in sliced and slit wafers,

or

- using instead cut wafers from a grown, arranged mono-crystal made from semiconductor material, making incisions at an angle approaching more or less 90° to the axial direction, according to a certain system and in a vertical direction to the wafer surface, cutting from the wafer edge

to a certain depth, but without cutting completely through the wafer,

and

- processing the slit wafers in each case by using generally known processing steps designed for such wafers, such as etching, mechanical and/or chemical-mechanical polishing, in order to obtain polished wafers,
- subjecting the polished wafers to a certain technological processing cycle, which includes high-temperature treatment and/or structuring (such as temper-hardening, oxidation, out-diffusion, in-diffusion, photolithography, etc.), then separating the structured wafers at the end of the processing cycle for optimum surface utilization, using abrasive cutting, notching and breaking, laser cutting, etc., in order to obtain separate components, which then can be bonded and encapsulated.

In accordance with the object of the invention, it is advantageous to make the incisions in the direction of the heat flows, which are generated during high-temperature treatment, that is, in a radial direction.

It is also in accordance with the object of the invention that, when determining the incision system, the symmetry of the voltage tensor, the generally rectangular shape of the component, and the crystallographic symmetry of the wafer must be taken into account; this means that preferably radial incision systems of a fourfold coordination should be used. In some cases an arranged radial incision will be sufficient to ensure that the improved characteristics of the wafer will be effective. If additional technical parameters are taken into consideration, non-radial incision systems may also be advantageous. Preferred directions for these incision systems are <211> for wafers with a (111) orientation, and <100> and <110> respectively for wafers with a (100) orientation.

In accordance with the described procedure it is preferable to remove sufficient material from the immediate incision area to ensure that the depth of interference caused by abrasive cutting is smaller than the thickness of the layer removed by etching, and that the mono-crystal or the wafer is heated only after the disturbed layer has been removed by an etching process. If this is not done, the surface defects of the crystal lattice (primarily dislocations) will be transferred to the wafer volume. Since it is technically less

difficult to make the incisions on the mono-crystal first, and then slice the mono-crystal into wafers, it would be advantageous to make sufficiently wide incisions on the grown mono-crystal, to enable an unobstructed area of attack for the etching agent, in order to ensure complete removal of the damaged layer, and then to etch the cut wafers, concluding with a mechanical/chemical-mechanical polishing process. This method ensures that the breaking-off of small pieces of material in the incision area which can cause scratches and abrasions during polishing of the wafer surface is effectively prevented. The invention is explained in the next chapter, using a simple embodiment.

Embodiment

FIG. 1 shows a diagram of a cut silicon wafer 1, produced according to the invention process (since the materials used for production as well as further processing and control procedures are part of the current state of technology, it is not necessary to illustrate such materials and steps). Wafer 1 has a diameter of 100 mm and a thickness of about 500 μm; it was cut by means of an inboard abrasive cutter from a CHOCHRALSKI-drawn silicon mono-crystal - known to be of the diamond lattice type - which was cut lengthwise with

an outboard abrasive cutter. Orientation of the surface normal line on the wafer runs approximately in the <111> direction, and the material is boron-doped from 4 to 8 Ω·cm. In the lower area of the wafer, chamfer 2 can be seen; normally, this cut is made on the mono-crystal before slicing, in order to facilitate the crystallographic orientation on the wafer. Starting from the center of chamfer 2 - that is, in a <110> direction, and offset by 90° each - four radial incisions 3, 4, 5 and 6 are made, which are each 25 mm deep and 1 mm wide; they represent the incision system and divide wafer 1 into the four sectors 7, 8, 9 and 10. The edges of the incisions 3, 4, 5 and 6, shown in FIG. 1 as borders, and the corners 11, 12, 13, 14, 15, 16, 17 and 18 are rounded off during the etching, prior to the polishing process. Under these conditions, the interference depth amounts to less than 20 μm. Correspondingly, the thickness of wafer 1 will be 400 μm after etching, and 380 μm after polishing. The incisions will widen to approximately 1,2 mm, since the slowest rate of material reduction will occur in the <111> direction. The polished wafer will be subjected to thermal oxidation at approximately 1450 K. The measured radii of curvature are on average considerably larger than for wafers having no incisions, made from

the same material and using current technology. Correspondingly, the structuring within the sectors 7, 8, 9 and 10 can be performed with the necessary precision; in addition, the remaining inaccuracies of the wafer shape exert only a minor influence, since the wafer produced according to the invention can be fitted more precisely during fixation for photolithographic processing. At the end of the so-called cycle I, which includes the high-temperature treatment to produce the actual electronic structures on the wafer, separation is performed by means of outboard abrasive cutting.

When using a different process in the sense of the invention, the incisions 3, 4, 5 and 6 can be made with varying depths; incision 3 in FIG. 1 could be extended to reach the center of the wafer, and incisions 4, 5 and 6 could be eliminated. Even with this modified incision system, reduced to just one incision, the projected advantages can be realized. The cutting effort is in this case particularly small, and there is minimal loss of structurable area. Since the incision itself makes orientation on the wafer possible, chamfering is probably not required when making incisions of variable depths or when using only one incision. This eliminates the processing steps and problems which occur during chamfering.

What is claimed is;

1. A method for producing special wafers made from semiconductor material; the production process includes already known manufacturing steps used in crystal growing, crystal separation, etching, mechanical and/or chemical-mechanical polishing, as well as temper-hardening, oxidation and/or diffusion,
characterized by

- growing a basically cylindrical mono-crystal made from semiconductor material by a known crystal-growing method, then making one or more incisions according to a certain system and in an axial direction, from the crystal shell to a certain depth, without cutting completely through the wafer;

- arranging the slit mono-crystal in such a way that it can be cut up at an angle approaching more or less 90° to the axial direction, resulting in sliced and slit wafers,

or using instead cut wafers from a grown, arranged mono-crystal made from semiconductor material, making incisions at an angle approaching more or less 90° to the axial direction, according to a certain system and in a vertical direction to the wafer surface, cutting from the wafer edge to a certain depth, but without cutting completely through the wafer,

and processing the slit wafers in each case by using generally known processing steps designed for such wafers, such as etching, mechanical and/or chemical-mechanical polishing, in order to obtain polished wafers,

and subjecting the polished wafers to a certain technological processing cycle, which includes high-temperature treatment and/or structuring (such as temper-hardening, oxidation, out-diffusion, in-diffusion, photolithography, etc.), then separating the structured wafers at the end of the processing cycle for optimum surface utilization, using abrasive cutting, notching and breaking, laser cutting, etc., in order to obtain separate components which then can be bonded and encapsulated.

2. Method according to Claim 1, characterized in that the incisions on the mono-crystal or the wafer are made in such a way that they correspond to the temperature field which is representative for the respective high-temperature treatment, that is, the incisions are arranged in the direction of the temperature gradient.

3. Method according to Claim 2, characterized in that the incisions are made in a radial direction.

4. Method according to Claim 1 or 3, characterized in that the incisions are made in a vertical direction to each other.

5. Method according to Claim 1 or 2, characterized in that the system of incisions (or the single incision) is made according to certain crystallographic arrangements.

6. Method according to Claim 5, characterized in that one of the incisions on wafers, which are obtained from a grown diamond-lattice type mono-crystal with a <111> orientation, is made in a <211> direction.

7. Method according to Claim 5, characterized in that one of the incisions on wafers, which are obtained from a grown diamond-lattice type mono-crystal with a <111> orientation, is made in a <110> direction.

8. Method according to Claim 5, characterized in that incisions on wafers, which are obtained from a grown diamond-lattice type mono-crystal with a <100> orientation, are made in <100> directions.

9. Method according to Claim 5, characterized in that incisions on wafers, which are obtained from a grown diamond-lattice type mono-crystal with a <100> orientation, are made in <110> directions.

10. Method according to Claims 4 and 6, characterized in that one of the four incisions on

wafers, which are obtained from a grown diamond-lattice type mono-crystal with a <111> orientation, is made in a <211> or <110> direction respectively.

11. Method according to Claim 4 and 8 or 4 and 9, characterized in that incisions on wafers, which are obtained from a grown diamond-lattice type mono-crystal with a <100> orientation, are made in <100> or <110> directions respectively.

12. Method according to Claim 1, characterized in that the reference direction for technological processes, such as during structuring of the wafer, is based on the incision system or a single incision instead of a chamfer.

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REISSUE APPLICATION DECLARATION BY THE ASSIGNEE

Docket Number (optional): 501.20289RC6

I hereby declare that:

My residence and post office address and citizenship are stated below next to my name.

I am authorized to act on behalf of the following assignee: HITACHI, LTD.

and the title of my position with said assignee is: Executive Managing Director

The entire title to the patent identified below is vested in said assignee.

Name of Patentee(s):

Hisashi Maejima, Hiroshi Nishizuka, Susumu Komoriya and Etuo Egashira

Patent Number	Date of Patent Issued
5,230,747	July 27, 1993

Title of Invention: WAFER HAVING CHAMFERED BEND PORTIONS IN THE JOINT REGIONS BETWEEN THE CONTOUR OF THE WAFER AND THE CUT-AWAY PORTION OF THE WAFER

I believe said patentee(s) to be the original, first and sole/joint inventor(s) of the subject matter which is described and claimed in said patent, for which a reissue patent is sought on the invention entitled WAFER HAVING CHAMFERED BEND PORTIONS IN THE JOINT REGIONS BETWEEN THE CONTOUR OF THE WAFER AND THE CUT-AWAY PORTION OF THE WAFER, the specification of which

☒ is attached hereto.

☐ was filed on _____ as reissue application number _____
and was amended on _____
(If applicable)

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.
Claim for priority - see page 3.
I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.
An Information Disclaimer Statement is filed herewith.
I verily believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☒ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☐ by reason of other errors.

At least one error upon which reissue is based is described as follows:

There is a mistake in the issued claims of the patent in that by a description of the issued claims, the purpose of providing a notch was unclear. The expression "curved notch" in claims 1 and 2 should be changed to -- curved positioning notch -- to clarify this and new claims 4-13 should be added. New claims 4-13 are not broadening the invention and were originally disclosed in the application, but applicant failed to notice the claiming in the application of U.S. Patent No. 5,230,747.

[Attach additional sheets, if needed.]

All errors corrected in this reissue application arose without any deceptive intention on the part of the applicant.

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(REISSUE APPLICATION DECLARATION BY THE ASSIGNEE, page 2)

Docket Number (Optional) 501.20289RC6

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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(and others on attached Addendum)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and imprisonment, or both, under 18 U.S.C. 1 001, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this declaration is directed.

Full name of person signing (given name, family name)
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PRIORITY CLAIM

I hereby claim foreign priority benefits under Title 35, United States Code, section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Such applications have been filed as follows:

EARLIEST FOREIGN APPLICATION(S), IF ANY FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO SAID APPLICATION

Country	Application No.	Date of filing (day, month, year)	Date of issue (day, month, year)	Priority claimed
Japan	570131949	30 July 1982		Yes

A D D E N D U M

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DECLARATION

REGISTERED PRACTITIONER INFORMATION (Supplemental Sheet)

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Noel B. Whitley	27,477		
Henry M. Zykorie			

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REISSUE APPLICATION BY THE ASSIGNEE, OFFER TO SURRENDER PATENT	Docket Number (Optional) 501.20289RC6

This is part of the application for a reissue patent based on the original patent identified below.

Name of Patentee(s): Hisashi MAEJIMA, Hiroshi NISHIZUKA, Susumu KOMORIYA and Etuo EGASHIRA

Patent Number	Date Patent Issued
5,230,747	July 27, 1993

Title of Invention: WAFER HAVING CHAMFERED BEND PORTIONS IN THE JOINT REGIONS BETWEEN THE CONTOUR OF THE WAFER AND THE CUT-AWAY PORTION OF THE WAFER

HITACHI, LTD. is the assignee of the entire interest in the original patent.
The assignment is recorded at Reel 4900, Frame 958.
I offer to surrender the original patent.

[X] A certificate under 37 CFR 3.73(b) is attached.

I am authorized to act on behalf of the assignee.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application, any patent issued thereon, or any patent to which this declaration is directed.

Name of assignee

HITACHI, LTD.

Signature of person signing for assignee	Date
Yasuo Sakuta	Oct. 17, 2000

Typed or printed name and title of person signing for assignee

Yasuo Sakuta, Executive Managing Director

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501.20289RC6

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): **H. MAEJIMA ET AL.**

Serial No. : **Not Assigned Yet**
(Reissue of Patent No.: 5,230,747
Issued: July 27, 1993)

Filed: **November 3, 2000**

For: **WAFER HAVING CHAMFERED BEND PORTIONS IN THE JOINT REGIONS BETWEEN THE CONTOUR OF THE WAFER AND THE CUT-AWAY PORTION OF THE WAFER**

REQUEST FOR TRANSFER OF DRAWINGS FROM ORIGINAL PATENT TO REISSUE APPLICATION

Assistant Commissioner of Patents
Washington, D.C. 20231

November 3, 2000

Sir:

Please transfer the drawings from original patent, 5,230,747, filed on July 27, 1993, for the invention entitled WAFER HAVING CAMFERED BEND PORTIONS IN THE JOINT REGIONS BETWEEN THE CONTOUR OF THE WAFER AND THE CUT-AWAY PORTION OF THE WAFER to the reissue application, the specification of which is attached hereto.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

Ronald J. Shore
Registration No. 28,577

RJS:alw
(703) 312-6600

FIG. 1

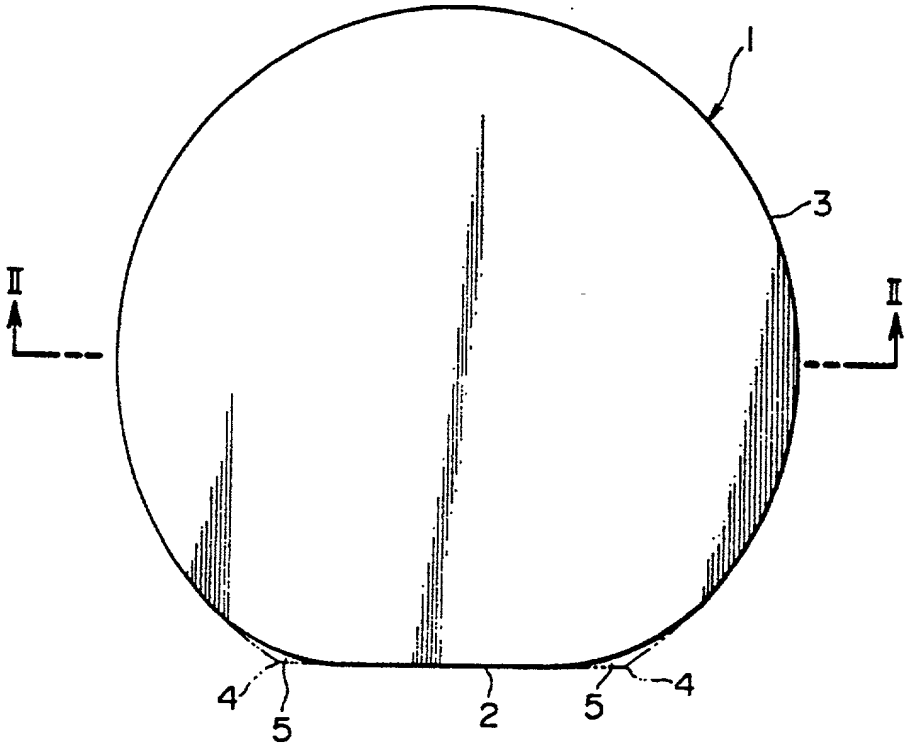

FIG. 2

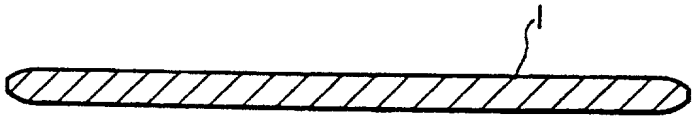

FIG. 3

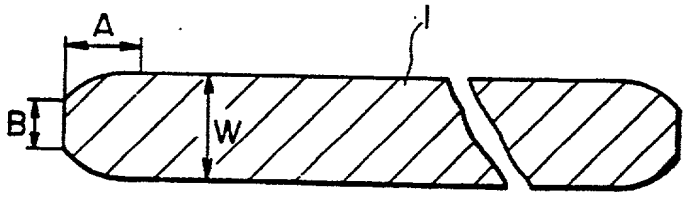

FIG. 4

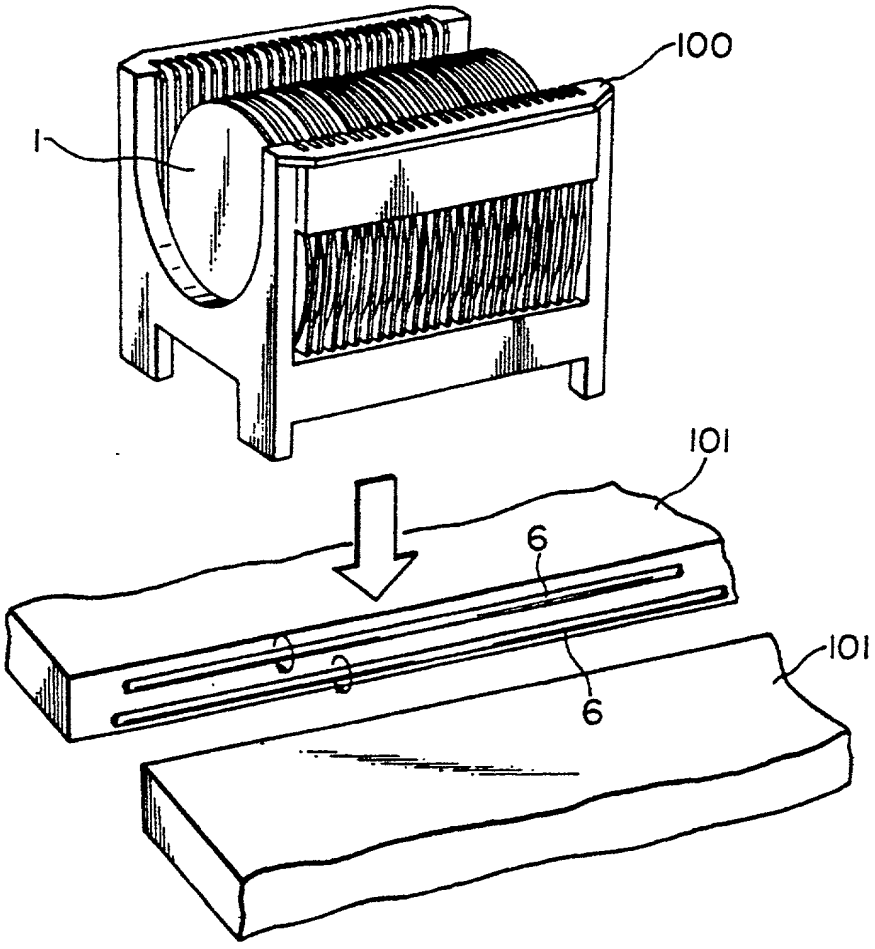

FIG. 5

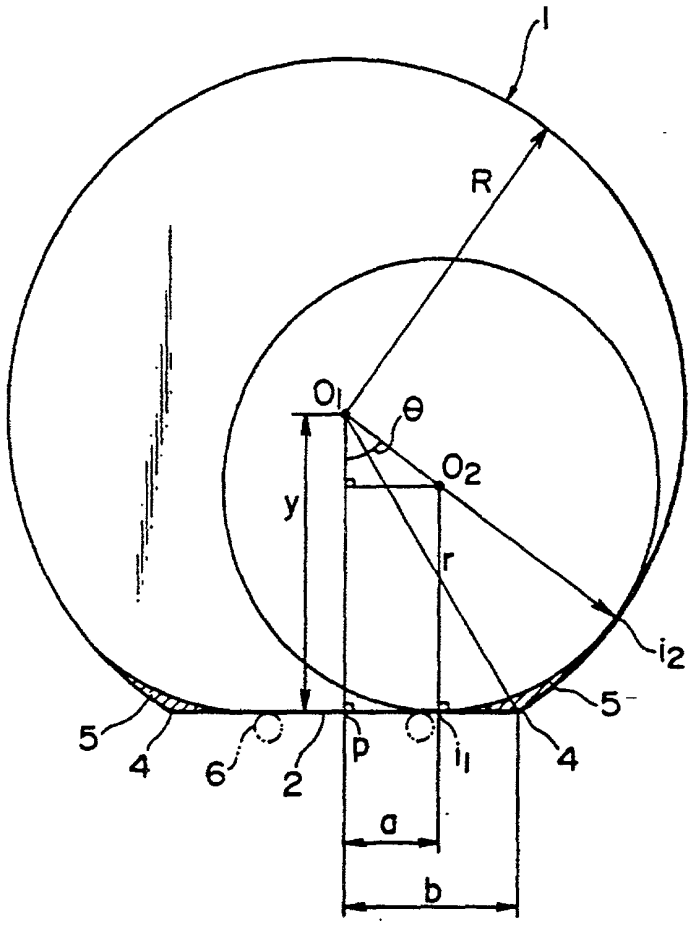

FIG. 6

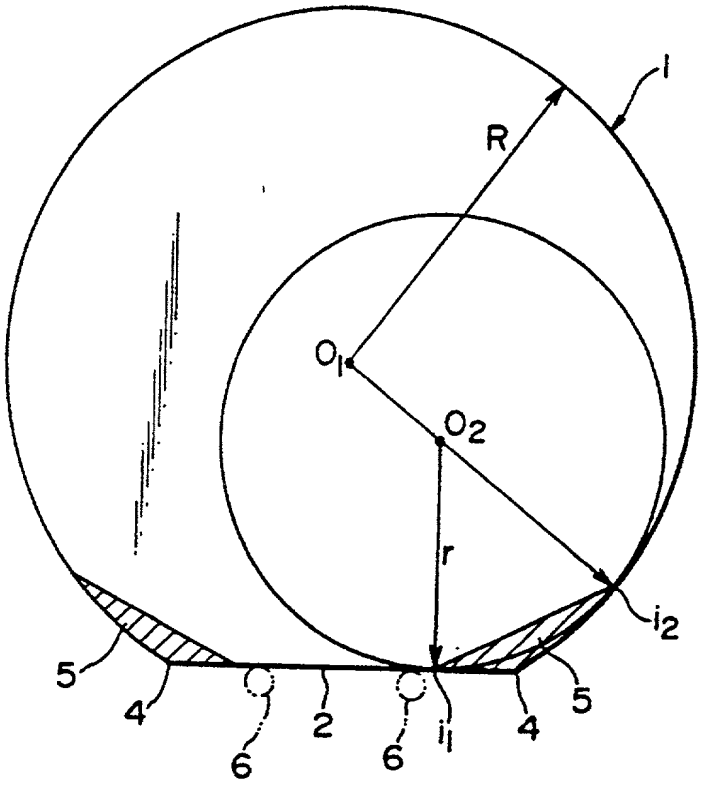

FIG. 7

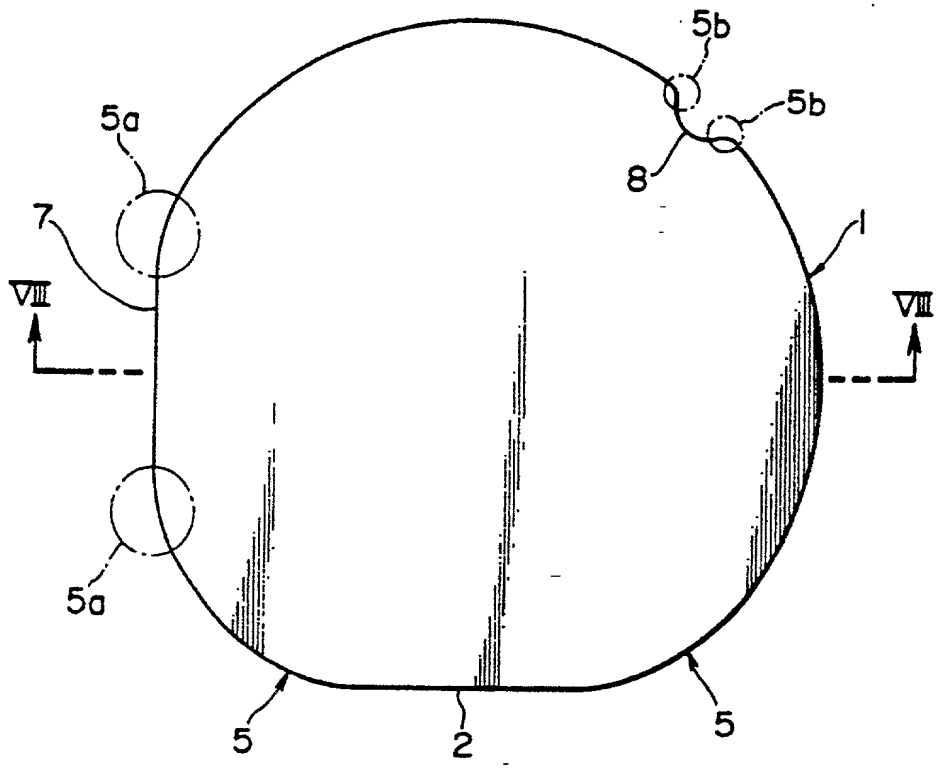

FIG. 8

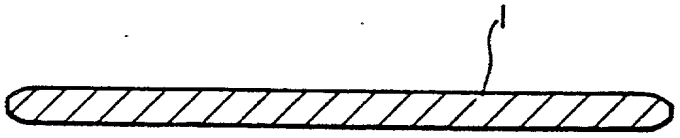

FIG. 9

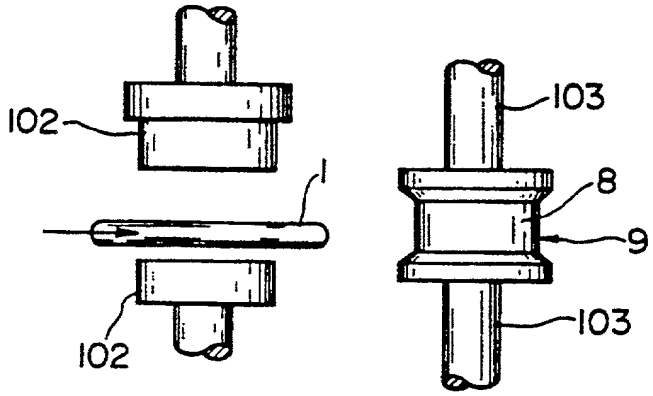

FIG. 10

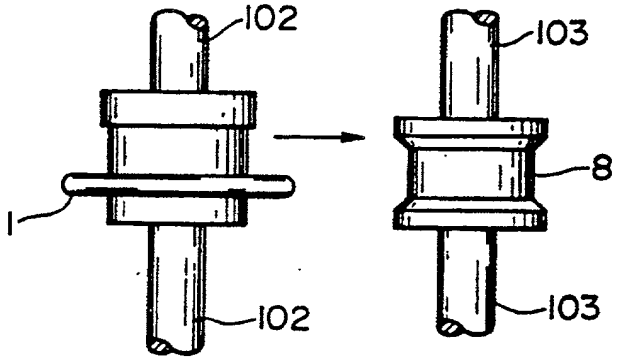

FIG. 11

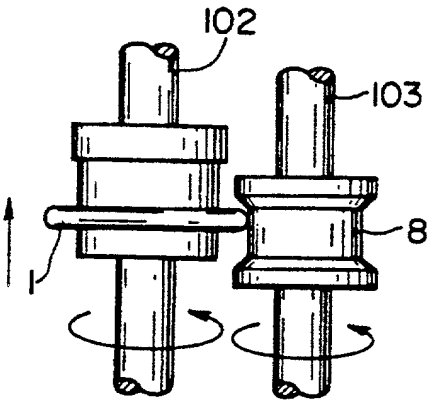

FIG. 12

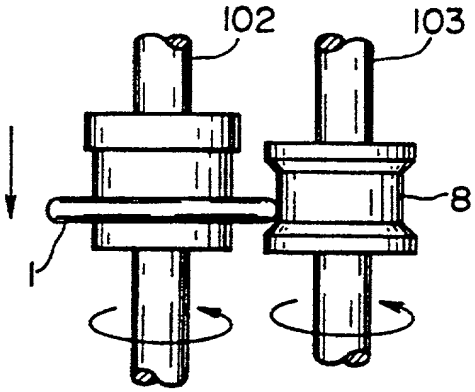

FIG. 13

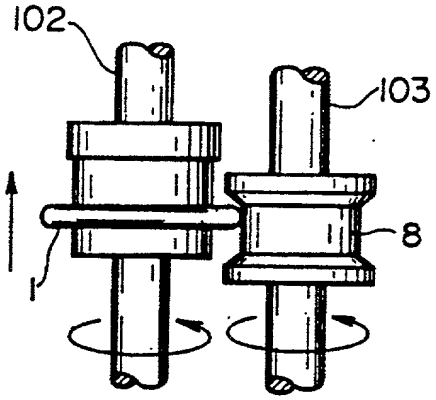

FIG. 14

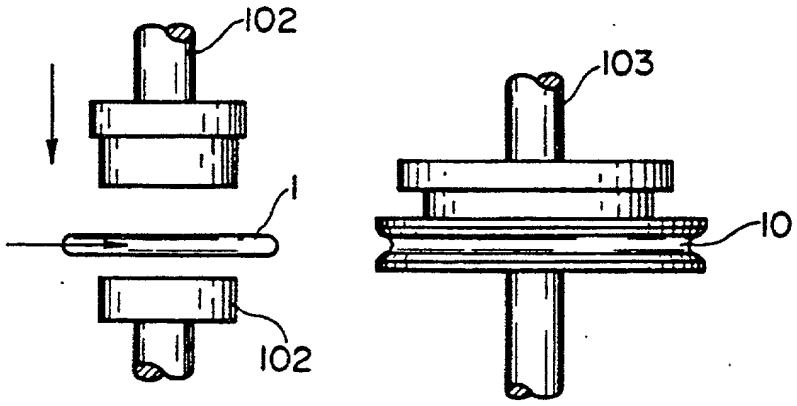

FIG. 15

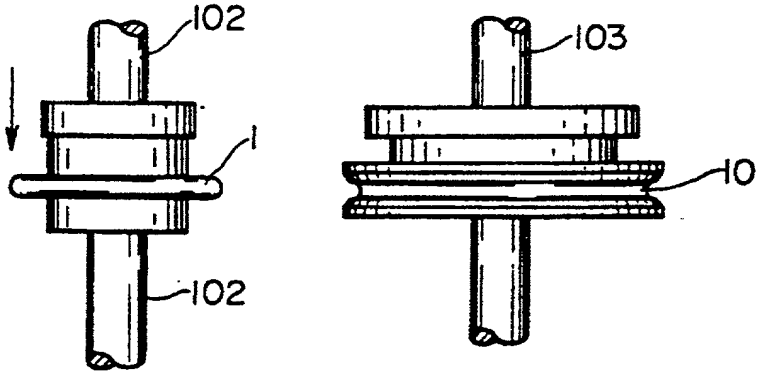

FIG. 16

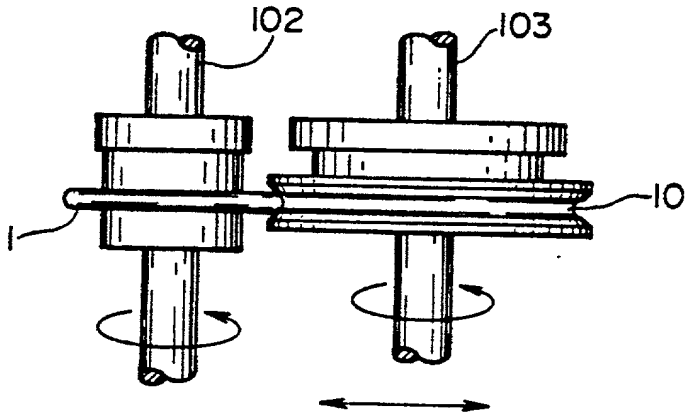

FIG. 17